

## FEATURES

- Provides six ultra-low skew copies of the selected input
- 2:1 MUX input included for clock switchover applications
- Guaranteed AC performance over temperature and voltage:
  - Clock frequency range: DC to > 6GHz
  - <290ps IN-to-OUT  $t_{pd}$
  - <60ps  $t_r / t_f$  times
  - <20ps skew (output-to-output)
- Unique input isolation design minimizes crosstalk
- Ultra low-jitter design:
  - <1ps<sub>RMS</sub> random jitter
  - <10ps<sub>PP</sub> total jitter (clock)
  - <1ps<sub>RMS</sub> cycle-to-cycle jitter
  - <0.7ps<sub>RMS</sub> crosstalk-induced jitter
- Low supply voltage operation: 2.5V and 3.3V
- Unique input termination and VT pin accepts DC-coupled and AC-coupled inputs (CML, PECL, LVDS)
- Internal 50 $\Omega$  output source termination
- 400mV CML output swing
- -40°C to +85°C temperature range
- Available in 32-pin (5mm x 5mm) MLF® package



Precision Edge®

## DESCRIPTION

The SY58034U is a 2.5V/3.3V precision, high-speed 1:6 fanout buffer capable of handling clocks up to 6GHz. A differential 2:1 MUX input is included for redundant clock switchover applications.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows the device to interface to any differential signal (AC- or DC-coupled) as small as 100mV without any level shifting or termination resistor networks in the signal path. The outputs are 50 $\Omega$  source terminated CML, with extremely fast rise/fall times guaranteed to be less than 60ps.

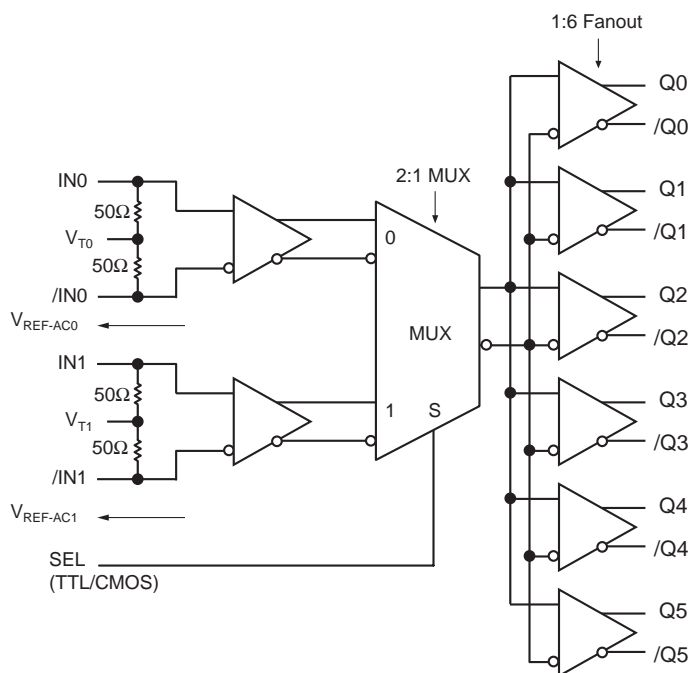
The SY58034U operates from a 2.5V  $\pm$ 5% supply or a 3.3V  $\pm$ 10% supply and is guaranteed over the full industrial temperature range of -40°C to +85°C. For applications that require LVPECL outputs, consider the SY58035U or SY58036U Multiplexers. The SY58034U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at [www.micrel.com](http://www.micrel.com).

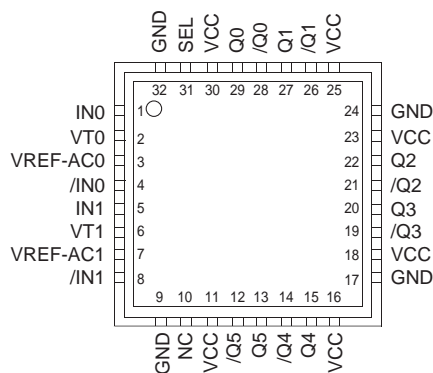
## APPLICATIONS

- Redundant clock distribution
- All SONET/SDH clock distribution
- All Fibre Channel distribution
- All Gigabit Ethernet clock distribution

## FUNCTIONAL BLOCK DIAGRAM



**PACKAGE/ORDERING INFORMATION**



**32-Pin MLF® (MLF-32)**

**Ordering Information(1)**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58034UMI	MLF-32	Industrial	SY58034U	Sn-Pb
SY58034UMITR <sup>(2)</sup>	MLF-32	Industrial	SY58034U	Sn-Pb
SY58034UMG <sup>(3)</sup>	MLF-32	Industrial	SY58034U with Pb-free bar-line indicator	NiPdAu Pb-Free
SY58034UMGTR <sup>(2, 3)</sup>	MLF-32	Industrial	SY58034U with Pb-free bar-line indicator	NiPdAu Pb-Free

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

**PIN DESCRIPTION**

Pin Number	Pin Name	Pin Function
1, 4 5, 8	IN0, /IN0 IN1, /IN1	Differential Input: These input pairs are the differential signal inputs to the device. These inputs accept AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the “Input Interface Applications” section for more details.
2, 6	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT0 and VT1 pins provide a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
31	SEL	This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. The MUX select switchover function is asynchronous.
10	NC	No connect.
11, 16, 18, 23, 25, 30	VCC	Positive Power Supply: Bypass with 0.1μF™™0.01μF low ESR capacitors and place as close to the VCC pins as possible.
29, 28 27, 26 22, 21 20, 19 15, 14 13, 12	Q0, /Q0, Q1, /Q1, Q2, /Q2, Q3, /Q3, Q4, /Q4, Q5, /Q5	Differential Outputs: These CML output pairs are low skew output copies of the selected input. The output stage is optimized to deliver a 400mV swing (single-ended) into 50Ω. Each output includes a 50Ω source-termination resistor, thus minimizing any return reflections. Unused output pins may be left floating. Please refer to the “Truth Table” for details.
9, 17, 24, 32	GND, Exposed Pad	Ground. Ground pin and exposed pad must be connected to the same ground plane.
3, 7	VREF-AC0, VREF-AC1	Reference Voltage: These output biases to V <sub>CC</sub> -1.2V. It is used for AC-coupling inputs (IN, /IN). Connect V <sub>REF-AC</sub> directly to the VT pin. Bypass with 0.01μF low ESR capacitor to V <sub>CC</sub> . See “Input Interface Applications” section. Maximum sink/source current is ±1.5mA. Due to the limited capability, the VREF-AC pin is only intended to drive its respective VT pin.

**TRUTH TABLE**

SEL	
0	IN0 Input Selected
1	IN1 Input Selected

### Absolute Maximum Ratings<sup>(1)</sup>

Power Supply Voltage ( $V_{CC}$ ) ..... -0.5V to +4.0V  
 Input Voltage ( $V_{IN}$ ) ..... -0.5V to  $V_{CC}$   
 CML Output Voltage ( $V_{OUT}$ ) .....  $V_{CC}-1.0V$  to  $V_{CC}+0.5V$   
 Termination Current  
     Source or sink current on VT pin .....  $\pm 100mA$   
 Input Current  
     Source or sink current on IN, /IN pin .....  $\pm 50mA$   
     Source or sink current on VREF-AC pin .....  $\pm 2mA$   
 Lead Temperature (soldering, 20 sec.) ..... 260°C  
 Storage Temperature Range ( $T_S$ ) ..... -65°C to +150°C

### Operating Ratings<sup>(2)</sup>

Power Supply Voltage ( $V_{CC}$ ) ..... +2.375V to +2.625V  
     ..... +3.0V to +3.6V  
 Ambient Temperature Range ( $T_A$ ) ..... -40°C to +85°C  
 Package Thermal Resistance<sup>(3)</sup>  
     MLF® ( $\theta_{JA}$ )  
         Still-Air ..... 35°C/W  
     MLF® ( $\Psi_{JB}$ )  
         Junction-to-Board ..... 16°C/W

## DC ELECTRICAL CHARACTERISTICS<sup>(4)</sup>

$T_A = -40^\circ C$  to  $85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply Voltage		2.375	2.5	2.625	V
			3.0	3.3	3.6	V
$I_{CC}$	Power Supply Current	No load, max. $V_{CC}$		245	320	mA
$R_{DIFF\_IN}$	Differential Input Resistance  IN-/IN		90	100	110	Ω
$R_{IN}$	Input Resistance (IN-to-VT)		45	50	55	Ω
$V_{IH}$	Input HIGH Voltage (IN, /IN)	<b>Note 5</b>	$V_{CC}-1.6$		$V_{CC}$	V
$V_{IL}$	Input LOW Voltage (IN, /IN)		0		$V_{IH}-0.1$	V
$V_{IN}$	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing  IN, /IN	See Figure 1b.	0.2			V
$V_{T\_IN}$	IN to $V_T$ (IN, /IN)				1.28	V
$V_{REF-AC}$	Reference Voltage		$V_{CC}-1.3$	$V_{CC}-1.2$	$V_{CC}-1.1$	V

**Notes:**

1. Permanent device damage may occur if the measurements in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes exposed pad is soldered (or equivalent) to the device’s most negative potential on the PCB.  $\Psi_{JB}$  and  $\theta_{JA}$  are determined for a 4-layer board in a still air, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5.  $V_{IH}$  (min) not lower than 1.2V.

**CML OUTPUT DC ELECTRICAL CHARACTERISTICS<sup>(6)</sup>**

$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $T_A = -40^\circ C$  to  $85^\circ C$ ;  $R_L = 100\Omega$  across each output pair or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage	$R_L = 50\Omega$ to $V_{CC}$	$V_{CC} - 0.020$		$V_{CC}$	V
$V_{OUT}$	Output Voltage Swing	See Figure 1a.	325	400		mV
$V_{DIFF\_OUT}$	Differential Output Voltage Swing	See Figure 1b.	650	800		mV
$R_{OUT}$	Output Source Impedance		40	50	60	$\Omega$

**LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS<sup>(6)</sup>**

$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $T_A = -40^\circ C$  to  $85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input HIGH Voltage		2.0			V
$V_{IL}$	Input LOW Voltage				0.8	V
$I_{IH}$	Input HIGH Current		-125		40	$\mu A$
$I_{IL}$	Input LOW Current		-300			$\mu A$

**Note:**

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**AC ELECTRICAL CHARACTERISTICS<sup>(7)</sup>**

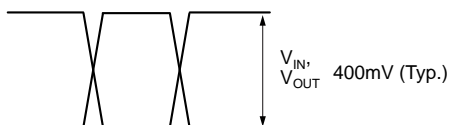
$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $T_A = -40^\circ C$  to  $85^\circ C$ ,  $R_L = 100\Omega$  across each output pair, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Operating Frequency	Clock $V_{OUT} \approx 200mV$	6	7.5		GHz
$t_{pd}$	Differential Propagation Delay (IN0 or IN1-to-Q) (SEL-to-Q)		140	220	290	ps
			100	200	400	ps
$\Delta t_{pd} Tempco$	Differential Propagation Delay Temperature Coefficient			65		fs/°C
$t_{SKEW}$	Output-to-Output	<b>Note 8</b>			20	ps
	Part-to-Part	<b>Note 9</b>			100	ps
$t_{JITTER}$	Clock	Cycle-to-Cycle Jitter	<b>Note 10</b>		1	ps <sub>RMS</sub>
		Random Jitter (RJ)	<b>Note 11</b>		1	ps <sub>RMS</sub>
		Total Jitter (TJ)	<b>Note 12</b>		10	ps <sub>PP</sub>
	Adjacent Channel Crosstalk-Induced Jitter	<b>Note 13</b>			0.7	ps <sub>RMS</sub>
$t_r, t_f$	Output Rise/Fall Time	Full swing, 20% to 80%	20		60	ps

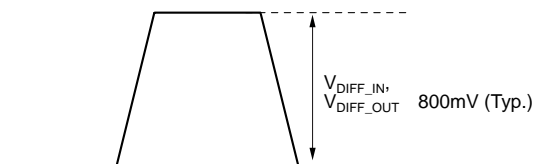
**Notes:**

- High frequency AC electricals are guaranteed by design and characterization.
- Output-to-output skew is measured between outputs under identical transitions.
- Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
- Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles,  $T_n - T_{n-1}$  where T is the time between rising edges of the output signal.
- Random jitter is measured with a K28.7 pattern, measured at 2.5Gbps.
- Total jitter definition: with an ideal clock input of frequency -  $f_{MAX}$ , no more than one output edge in  $10^{12}$  output edges will deviate by more than the specified peak-to-peak jitter value.
- Crosstalk is measured at the output while applying two similar clock frequencies that are asynchronous with respect to each other at the inputs.

**SINGLE-ENDED AND DIFFERENTIAL SWINGS**

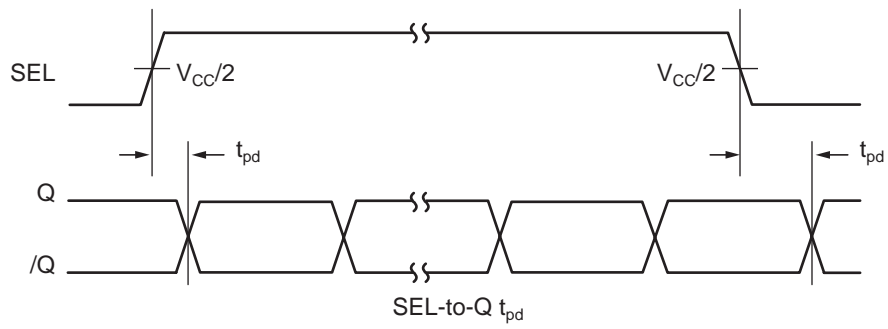
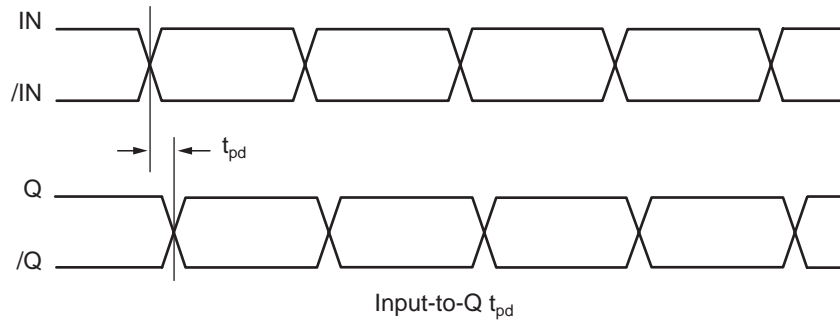


**Figure 1a. Single-Ended Voltage Swing**



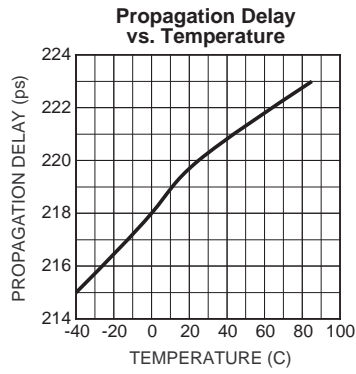
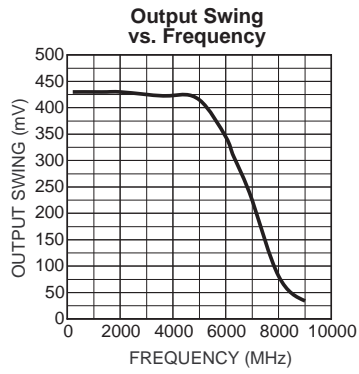
**Figure 1b. Differential Voltage Swing**

**TIMING DIAGRAMS**



**TYPICAL OPERATING CHARACTERISTICS**

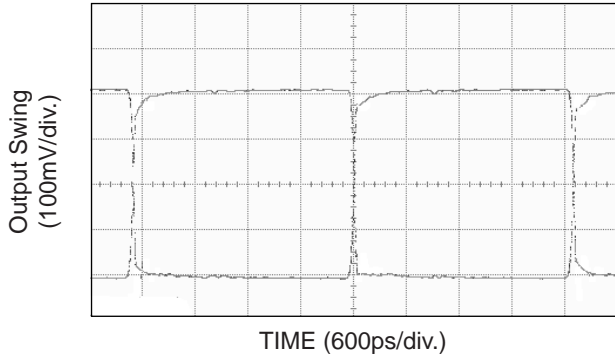
$V_{CC} = 2.5V$ ,  $GND = 0$ ,  $V_{IN} = 100mV$ ,  $R_L = 100\Omega$  across the output;  $T_A = 25^\circ C$ , unless otherwise stated.



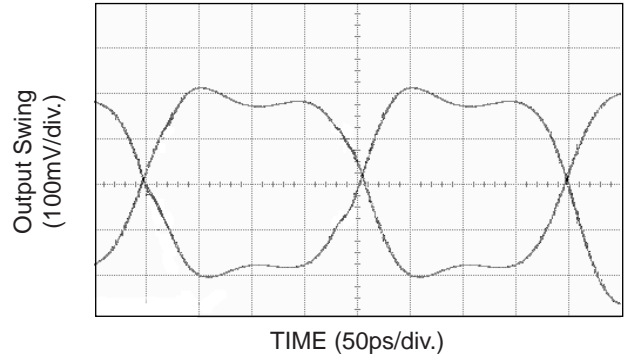
# FUNCTIONAL CHARACTERISTICS

$V_{CC} = 2.5V$ ,  $GND = 0$ ,  $V_{IN} = 400mV$ ,  $R_L = 100\Omega$  across the output;  $T_A = 25^\circ C$ , unless otherwise stated.

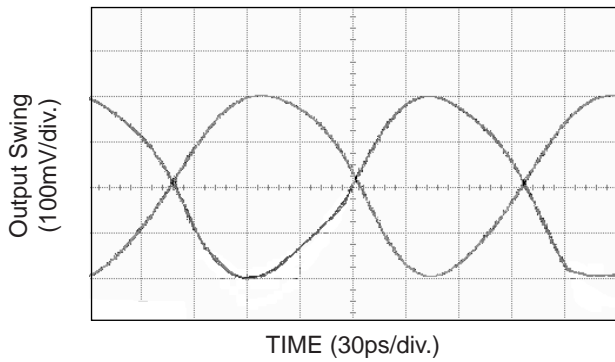
200MHz Output



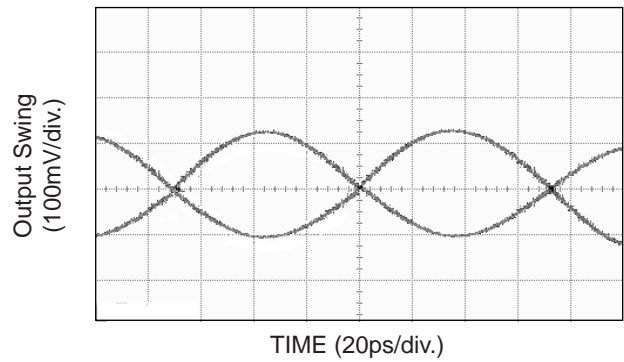
2.5GHz Output



5GHz Output



7GHz Output





**INPUT AND OUTPUT STAGES**

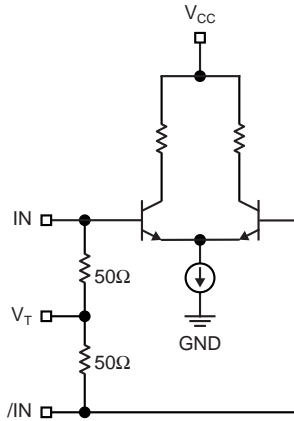


Figure 2a. Simplified Differential Input Stage

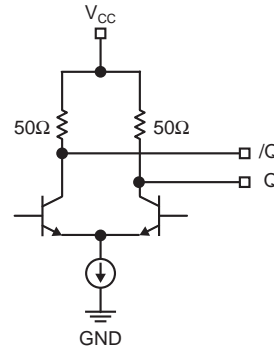


Figure 2b. Simplified CML Output Stage

**INPUT INTERFACE APPLICATIONS**

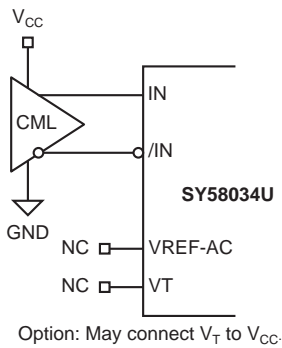


Figure 3a. CML Interface (DC-Coupled)

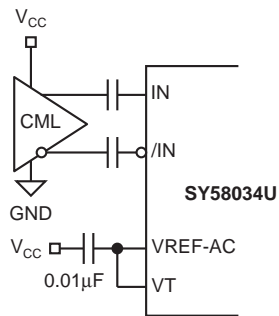


Figure 3b. CML Interface (AC-Coupled)

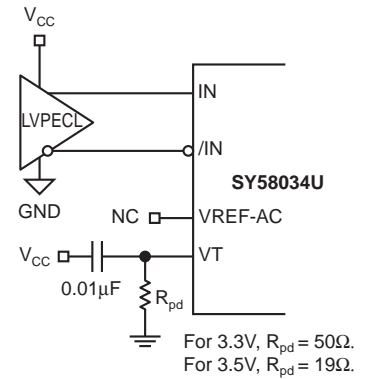


Figure 3c. LVPECL Interface (DC-Coupled)

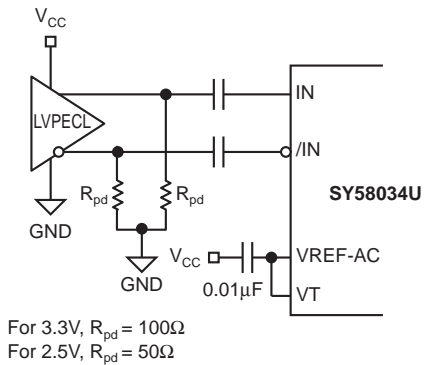


Figure 3d. LVPECL Interface (AC-Coupled)

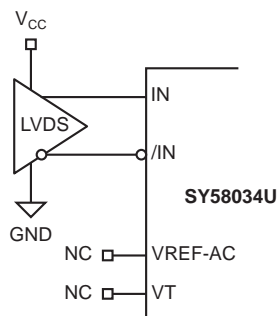
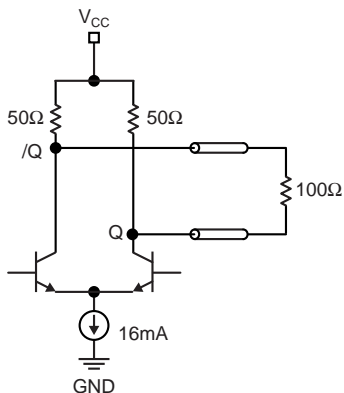
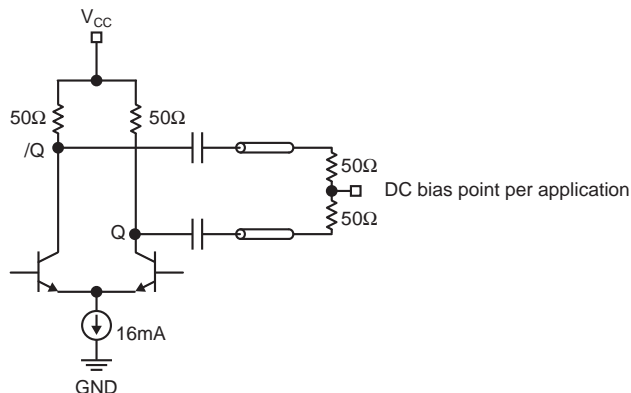


Figure 3e. LVDS Interface

**OUTPUT INTERFACE APPLICATIONS**



**Figure 4. CML DC-Coupled Termination**

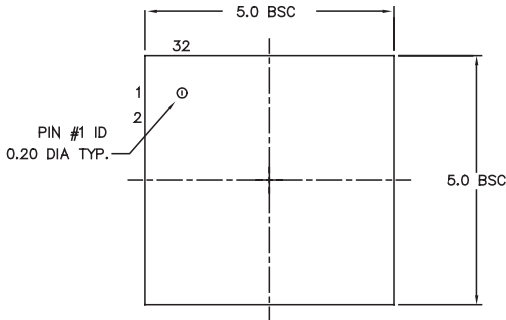


**Figure 5. CML AC-Coupled Termination**

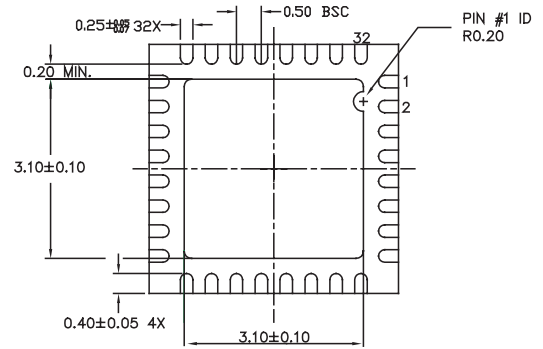
**RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION**

Part Number	Function	Data Sheet Link
SY58035U	4.5GHz, 1:6 LVPECL Fanout Buffer with 2:1 MUX Input and Internal Termination	<a href="http://www.micrel.com/product-info/products/sy58035u.shtml">http://www.micrel.com/product-info/products/sy58035u.shtml</a>
SY58036U	6GHz, 1:6 400mV LVPECL Fanout Buffer with 2:1 MUX Input and Internal Termination	<a href="http://www.micrel.com/product-info/products/sy58036u.shtml">http://www.micrel.com/product-info/products/sy58036u.shtml</a>
	MLF® Application Note	<a href="http://www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf">www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf</a>
HBW Solutions	New Products and Applications	<a href="http://www.micrel.com/product-info/products/solutions.shtml">www.micrel.com/product-info/products/solutions.shtml</a>

**32-PIN MicroLeadFrame® (MLF-32)**



TOP VIEW



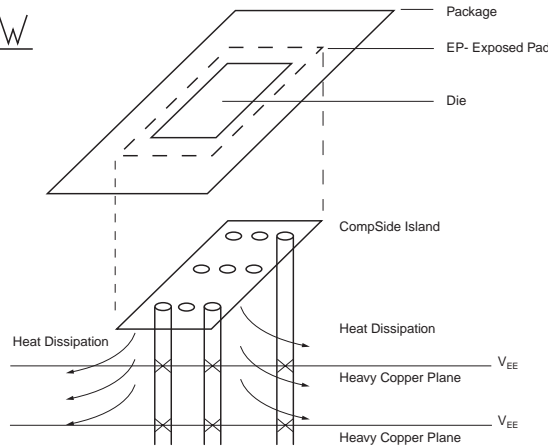
BOTTOM VIEW



SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



**PCB Thermal Consideration for 32-Pin MLF® Package  
(Always solder, or equivalent, the exposed pad to the PCB)**

**Package Notes:**

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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